11-20-00 A

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE
UTILITY PATENT APPLICATION TRANSMITTAL LETTER

Attorney Docket No.: SC0822ET

To: Assistant Commissioner for Patents
Box Patent Application
Washington D.C., 20231

Dear Assistant Commissioner:

Transmitted herewith for filing under 37 C.F.R. §1.53(b) is a Nonprovisional Utility Patent Application for a New Application entitled:

METHOD OF FORMING A DIODE FOR INTEGRATION WITH A SEMICONDUCTOR DEVICE AND METHOD OF FORMING A TRANSISTOR DEVICE HAVING AN INTEGRATED DIODE by:

Jean-Michel Reynes et al.

The filing fee is calculated as follows:

CLAIMS AS FILED AFTER AMENDING THE APPLICATION
AS SET FORTH IN THE PARAGRAPHS BELOW

FOR	NUMBER OF CLAIMS	NUMBER EXTRA	RATE	FEE
TOTAL CLAIMS	9 - 20 =	0	x $18 =	$ 00.00
INDEPENDENT CLAIMS	2 - 3 =	0	x $80 =	0.00
MULTIPLE DEPENDENT CLAIMS			$270	0.00
BASIC FEE				710.00
TOTAL FILING FEE				$ 710.00

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Express Mail Label No. EL581727333US

Attorney Docket No.: SC0822ET

Enclosed are:

_X_ 3 sheets of drawings and 11 pages of specification.

_X_ Unsigned Combined Declaration and Power of Attorney.

_____ Copy of declaration from prior United States Patent Application No. _____ filed on _____.

_X_ A paper entitled "Authorization for Fees Under 37 C.F.R. §§1.16 and 1.17 and Petitions for Extensions of Time."

_____ A Recordation Form Cover Sheet and an Assignment of the invention.

_____ Preliminary amendment.

_____ Enter the unentered 37 C.F.R. §1.116 amendment filed in the prior application.

_____ Information Disclosure Citation (Form PTO-1449) and copies of the cited references therein (other than pending U.S. patent applications) are enclosed.

_X_ A Return Postcard specifically listing all enclosures.

_____ Incorporation by Reference (for Continuation/Division application). The entire disclosure of the prior application, from which a copy of the oath or declaration is supplied, is considered as being part of the disclosure of the accompanying application and is hereby incorporated by reference therein. Because the present application is based on a prior U.S. patent application, please amend the specification by adding the following sentence before the first sentence of the specification:

"This is based on prior United States Patent Application No. 09/000,000, filed on January 1, 1999, which is hereby incorporated by reference, and priority thereto for common subject matter is hereby claimed."

_____ Cancel claims _____ of the prior application before calculating the filing fee.

_X_ Priority of patent application number 99402846.2 filed on November 17, 1999 in EPC is hereby claimed under 35 U.S.C. §119.

A certified copy of the foreign patent application has previously been sent.

_____ Priority of U.S. Patent Application No. _____ filed on _____ is hereby claimed under 35 U.S.C. §119(e).

_____ Priority of U.S. Patent Application No. _____ filed on _____ is hereby claimed under 35 U.S.C. §120.

_____ This Application is being filed by fewer than all the inventors named in the prior application. Amend the current Application by deleting the following inventors pursuant to 37 C.F.R. §1.53: _____.

_____ An assignment has been previously submitted and recorded.

_____ Other:

Please forward all correspondence to:

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11/17/00
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METHOD OF FORMING A DIODE FOR INTEGRATION WITH A SEMICONDUCTOR DEVICE AND METHOD OF FORMING A TRANSISTOR DEVICE HAVING AN INTEGRATED DIODE

Field of the Invention

This invention relates to a method of forming a diode for integration with a semiconductor device and a method of forming a transistor device having an integrated diode.

Background of the Invention

The use of a diode integrated with a semiconductor device, such as a power MOSFET device, as an integrated temperature sensor is well known. For example, the forward voltage of the diode is proportional to the temperature of the diode and so by monitoring the forward voltage across a diode integrated with a power device, the temperature of the power device can be monitored which is useful, for example, when tracking the device's temperature overshoot and subsequent shutdown.

Typically, an integrated diode is formed by doping a polysilicon layer with P-type and N-type dopants so as to form the diode's P/N junction. Although some of the process steps of forming such a polysilicon diode can be combined with the other processing steps for the semiconductor device, the known techniques all suffer from the disadvantage of requiring some additional process steps, e.g. additional masking steps for the P-type and N-type implant, and additional P-type and N-type implant steps, to create the diode. Additional process steps increase the complexity and cost of manufacture and provide additional opportunity for defects, which reduce the overall yield from such processes and reliability of the final product.

Brief Description of the Drawings

A method of forming a diode for integration with a semiconductor device will now be described, by way of example only, with reference to the accompanying drawings in which:

FIGs. 1-4 show simplified schematic cross-sectional diagrams of a diode during various stages of fabrication in accordance with the present invention; and

FIGs. 5-11 show simplified schematic cross-sectional diagrams of a transistor device having an integrated diode in accordance with the present invention during various stages of fabrication.

Detailed Description of the Drawings

A method of forming a diode in accordance with the present invention for integration with a semiconductor device will now be described with reference to FIGs. 1-4. To avoid complexity, the details of the semiconductor device have been omitted from FIGs. 1-4. It will be appreciated that the steps used in the following process may be used in conjunction with and as part of the process operations for the fabrication of the semiconductor device. An example of such a semiconductor device and process is briefly described below with reference to FIGs. 5-11. The example described herein is the process flow for a MOSFET transistor device. It will be appreciated that the present invention may be used with any semiconductor device requiring an integrated diode e.g. IGBT devices.

Although in the following description the layers and regions will be described as having certain conductivity types and being comprised of certain materials, this is for illustrative purposes only. It is not intended that the invention be limited to the specific conductivity types or the specific materials referred to herein.

Referring firstly to FIG. 1, a layer 4 of semiconductor material, which is preferably an N conductivity type epitaxial layer, is provided. A dielectric layer 6 is formed over the epitaxial layer 4. In the preferred embodiment, the dielectric layer 6 is an oxide layer having a thickness of 0.6 microns. A P conductivity type

dopant is then introduced into the dielectric layer 6, for example, by implantation of boron B11 or boron di-fluoride BF2 or other P-type dopant.

After the implantation step, a semi-conductive layer 8 is formed over the doped dielectric layer 6, FIG. 2. Preferably, the semi-conductive layer 8 is a layer of polysilicon material or oxygen doped polycrystalline silicon (SIPOS) material deposited on the dielectric layer 6 by standard deposition techniques. The P-type implantation parameters are selected such that the concentration of P conductivity type dopant in the subsequently outdiffused semi-conductive layer 8 is sufficient to ensure a good ohmic contact with a diode. This is typically at least 1 E18 atoms per cm^{-3}.

A photoresist mask 10 is then formed over the semi-conductive layer 8 and is patterned to expose a first region 12 of the semi-conductive layer 8. An N conductivity type dopant is then introduced into the semi-conductive layer 8, for example, by implantation of phosphorous, arsenic or other N conductivity type dopant (see FIG. 3). The implantation parameters are selected such that the concentration of N conductivity type dopant in the first region 12 of the semi-conductive layer 8 is sufficient to ensure a good ohmic contact between the N doped first region 12 and a diode contact. This is typically around 5-6 E19 atoms per cm^{-3}.

The mask 10 is then removed.

A cap layer 14 is formed over the semi-conductive layer 8, FIG. 4. Cap layer 14 typically comprises at least one dielectric layer and preferably comprises an oxide/nitride/oxide sandwich. The structure is then treated such that the P conductivity type dopant in the dielectric layer 6 is re-distributed into the semi-conductive layer 8 such that a second region 18 of P conductivity type is formed in the semi-conductive layer 8. The second region 18 corresponds to the region protected by the photoresist mask 10 from the N conductivity type implantation. In the preferred embodiment, for re-distribution of the dopants or out-diffusion of the dopants, the device is subjected to a high temperature heat treatment, for example, the device is heated to a temperature of greater than 1000 ºC for two hours. During the re-distribution step, some of the P conductivity type dopant also diffuses into the first region 12 and some of the N conductivity type dopant diffuses into the second region 18 but in the first region 12, N is the majority carrier and in the second region 18, P is the majority carrier. The first 12 and

second 18 regions are adjacent one another and provide the P/N junction of the integrated diode 2.

First and second openings are then formed in the cap layer 14 such that they extend to the first 12 and second 18 regions of the semi-conductive layer, respectively. Metal contacts are then formed in the first and second openings to the first 12 and second 18 regions of the semi-conductive layer to provide the diode contacts 16.

The invention has been described starting with a blanket P conductivity type implantation step followed by an N conductivity type implantation step into the semi-conductive layer. Alternatively, an N conductivity type blanket implantation step could be used followed by a P conductivity type implantation step into the semi-conductive layer. Good ohmic contacts are required between the first 12 and second 18 regions of the semi-conductive layer 8 and the contacts 16. To ensure a good ohmic contact a higher concentration of N dopant is needed in the N type region compared to the concentration of P dopant in the P type region. This means that although it is possible to start with a blanket N type implantation, a blanket P type implantation is preferred.

The present invention thus provides a method for forming a diode integrated with a semiconductor device wherein the P and N regions of the device are formed by one blanket implant step into a dielectric layer, one implant step into a semi-conductive layer, such as a polysilicon layer, with a mask and a re-distribution step wherein the dopant from the dielectric layer is out-diffused into the polysilicon layer. The blanket implant and re-distribution step avoids the need for an additional implant and extra mask. This can provide significant cost savings for the final product.

The present invention will now be described with reference to the fabrication of a particular type of semiconductor device having an integrated diode in accordance with the present invention. In the following description the semiconductor device is a High Density MOSFET device. Not all the steps are shown for simplicity. The fabrication of such devices are well known in the art. Like components to those of FIGs. 1-4 are referenced by the same reference numeral plus 100.

Referring now to FIG. 5, a first dielectric layer 106 is formed over a layer 104 of semiconductor material, which in the preferred embodiment is an N type

epitaxial layer. The epitaxial layer 104 is formed over an N-type substrate 103. In the preferred embodiment, the dielectric layer 106 is an oxide layer having a thickness of 0.6 microns. A P conductivity type dopant is then introduced into the oxide layer 106, for example, by implantation of boron B11 or boron di-fluoride BF2 or other P-type dopant.

The doped oxide layer 106 is patterned so as to provide an opening 105 in the oxide layer 106 extending to the epitaxial layer 104 (FIG. 6). The opening 105 forms an active area 105 of the transistor device. A second dielectric layer 107 having a thickness of 0.04 microns is formed on the epitaxial layer 104 in the active area 105. Preferably this second dielectric layer 107 is an oxide layer 107 formed by thermal diffusion. The second dielectric layer 107 is a gate oxide layer 107.

In FIG. 7, a semi-conductive layer 108, such as a polysilicon layer, is formed over the oxide layer 106 and the gate oxide layer 107. The polysilicon layer 108 has a thickness of approximately 0.5 microns and may be formed by deposition such as Low Pressure Chemical Vapour Deposition (LPCVD). A photoresist mask is deposited on the polysilicon layer 108 and patterned to leave a portion 109 on the polysilicon layer 108 over the oxide layer 106. The portion 109 protects a region of the polysilicon layer 108 which will become a diode region 118 of the integrated diode.

An N conductivity type dopant is then introduced into the polysilicon layer 108, for example, by implantation of phosphorous, arsenic or other N conductivity type dopant. As an example, a dose of 5 E15 atom per cm^{-3} of phosphorous at an energy of 50keV may be used for the N-type implantation step. The mask portion 109 ensures that the region of the polysilicon layer 108 underneath the mask portion 109 is not doped with phosphorous. After the implantation step, the mask portion 109 is removed. A portion of the N-type doped polysilicon layer 108 forms the polysilicon gate of the MOSFET device.

A cap layer 114 is then formed over the polysilicon layer 108 (FIG. 8). The cap layer 114 may comprise a combination of oxide/nitride/oxide layers formed by deposition and is used to provide protection against contamination. Openings 115 and 117 are then formed in the cap layer 114, polysilicon layer 108 to the gate oxide layer 107 in the active area 105 to define the gate. In the same process step, openings 161 (only one of which is shown in FIG. 8) are formed in

the cap layer 114 and the polysilicon layer 108 to the oxide layer 106 to isolate the diode from the rest of the polysilicon layer 108.

A P conductivity type dopant is then introduced into the epitaxial layer 104 through the openings 115 and 117 by, for example, implanting boron B11 at a dose in the range of 1E14 cm^{-2}. The cap layer 114 prevents the P-type dopant from being implanted into the polysilicon layer 108. After the implant, the device is heated to approximately 1100 ºC for two hours to drive the P-type dopant into the epitaxial layer 104 to form PHV regions 119 and 121 as shown in FIG. 9. During the heat treatment, the P-type dopant in the oxide layer 106 is re-distributed into the polysilicon layer 108 such that a P-type region 118 is formed in the polysilicon layer 108 adjacent a N-type region 112 in the polysilicon region 108. These N-type region and P-type region form the diode regions of an integrated diode 102.

In FIG. 10, a block mask 129 is formed in opening 117. An N conductivity type dopant is then introduced into the PHV regions 119 and 121 by, for example, implanting arsenic at a dose in the range of 1E16 cm^{-2} to form N-type regions 123, 125 and 127 in the PHV regions 119 and 121. N-type region 123 forms the source region of the MOSFET device.

A dielectric layer is deposited and etched to form spacers 150 in the openings 115, 117 and 161. A blanket P-type implant, followed by a thermal anneal is used to form body regions 152, 154 (FIG.11).

Openings are then formed in the cap layer 114 to the polysilicon layer 108 for the gate contact and the diode contacts. Metal is then deposited over the device, masked and etched to leave the source contact 131, gate contact 133 and diode contacts 116.

Although not shown in FIGs. 5-11, a drain contact is made to the backside of the device.

FIG. 11 shows a diode 102 integrated with a MOSFET transistor 135. In summary, diode 102 is formed by utilising a blanket P-type implantation step for implanting P-type dopant into the oxide layer 106, using the N-type implantation step which is used to form the polysilicon gate of the MOSFET device to form the N-type region 112 of the diode 102 and out-diffusing the P-type dopant from the oxide layer into a region of the polysilicon layer 108 to form the P-type region of the diode 102. The diode contacts are formed during the step of forming the gate

contact. Thus, only an additional blanket implant step and a single mask must be added to the standard MOSFET process to form the integrated diode 102. Compared to the prior art technique which requires a mask and an implant for each diode region, the present invention provides significant cost savings.

By performing the P-type blanket implantation before etching the oxide layer 106, this ensures that no p-type dopant diffuses through the gate oxide 107 into the epitaxial layer 104 or the polysilicon layer 108 in the active area 105 which can adversely affect the on-resistance Rdson of the MOSFET device. In other words, out-diffusion of the P-type dopant occurs in the oxide layer 106 only and not in the gate oxide layer 107.

Claims

1. A method of forming a diode for integration with a semiconductor device comprising the steps of:

providing a layer of semiconductor material;

forming a dielectric layer over the layer of semiconductor material;

introducing a first conductivity type dopant into the dielectric layer;

forming a semi-conductive layer over the dielectric layer;

introducing a second conductivity type dopant into a first region of the semi-conductive layer; and

re-distributing the first conductivity type dopant from the dielectric layer into the semi-conductive layer so as to form a second region of the first conductivity type dopant in the semi-conductive layer, the second region being adjacent the first region so as to provide a P/N junction of the diode.

2. The method according to claim 1 wherein the re-distributing step comprises heating the semiconductor device to diffuse the first conductivity type dopant into the semi-conductive layer.

3. The method according to claim 1 wherein the step of providing a layer of semiconductor material comprises the step of providing an epitaxial layer.

4. The method according to claim 1 further comprising the steps of:

forming a cap layer over the semi-conductive layer;

forming first and second openings in the cap layer extending to the first and second regions of the semi-conductive layer; and

forming contacts in the first and second openings to the first and second regions of the semi-conductive layer.

5. The method according to claim 4 wherein the step of forming a cap layer occurs before the re-distributing step.

6. The method according to claim 4 wherein the cap layer comprises at least one dielectric layer.

7. The method according to claim 1 wherein the step of forming a semi-conductive layer comprises the step of forming a layer of one of the following materials: polysilicon, and oxygen doped polycrystalline silicon (SIPOS).

8. The method according to claim 1 wherein the step of introducing a second conductivity type dopant comprises the steps of:

forming a mask over the semi-conductive layer;

removing a portion of the mask so as to expose the first region of the semi-conductive layer; and

implanting the second conductivity type dopant into the first region of the semi-conductive layer.

9. A method of forming a transistor device having an integrated diode, the method comprising the steps of:

providing a layer of semiconductor material;

forming a first dielectric layer over the layer of semiconductor material having a first thickness;

introducing a first conductivity type dopant into the first dielectric layer;

patterning the first dielectric layer so as to provide an opening in the first dielectric layer extending to the layer of semiconductor material, the opening forming an active area of the transistor device;

forming a second dielectric layer over the layer of semiconductor material in the active area having a second thickness, the first thickness being greater than the second thickness;

forming a semi-conductive layer over the first and second dielectric layers;

introducing a second conductivity type dopant into the semi-conductive layer over the active area and into a first region of the semi-conductive layer over the first dielectric layer;

forming a cap layer over the non-conductive region;

forming openings extending through the cap layer, and semi-conductive layer to the second dielectric layer in the active area and to the first dielectric layer;

introducing a dopant of the first conductivity type into the layer of semiconductor material through the openings in the active area;

re-distributing the first conductivity type dopant from the first dielectric layer into the semi-conductive layer over the first dielectric layer so as to form a second region of the first conductivity type dopant in the semi-conductive layer, the second region being adjacent the first region so as to provide a P/N junction of the integrated diode and re-distributing the dopant of the first conductivity type in the layer of semiconductor material so as to form regions of the first conductivity type in the semiconductor material;

introducing a dopant of the second conductivity type into the regions of the first conductivity type to form a source region of the transistor device; and

forming contacts to the source region, and the first and second regions.

METHOD OF FORMING A DIODE FOR INTEGRATION WITH A SEMICONDUCTOR DEVICE AND METHOD OF FORMING A TRANSISTOR DEVICE HAVING AN INTEGRATED DIODE

Abstract of the Disclosure

The present invention relates to a method of forming a diode (2) for integration with a semiconductor device comprising the steps of providing a layer (4) of semiconductor material, forming a dielectric layer (6) over the layer of semiconductor material, introducing a first conductivity type dopant into the dielectric layer (6), forming a semi-conductive layer (8) over the dielectric layer (6), introducing a second conductivity type dopant into a first region (12) of the semi-conductive layer and re-distributing the first conductivity type dopant from the dielectric layer (6) into the semi-conductive layer (8) so as to form a second region (18) of the first conductivity type dopant in the semi-conductive layer (8), the second region (18) being adjacent the first region (12) so as to provide a P/N junction of the diode (2).

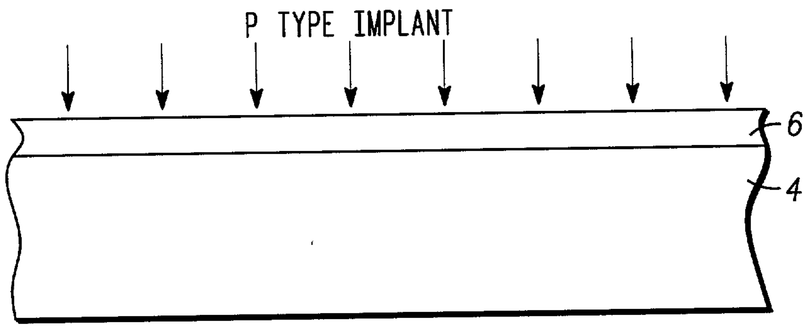

FIG. 1

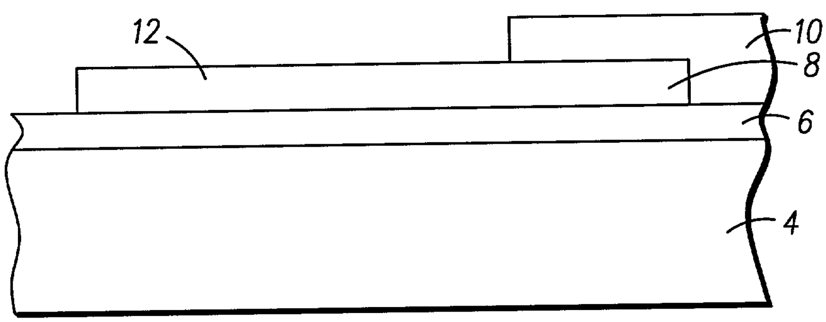

FIG. 2

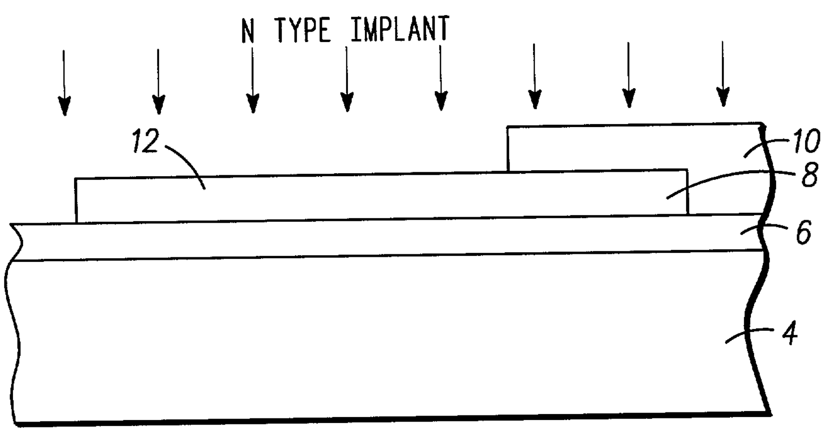

FIG. 3

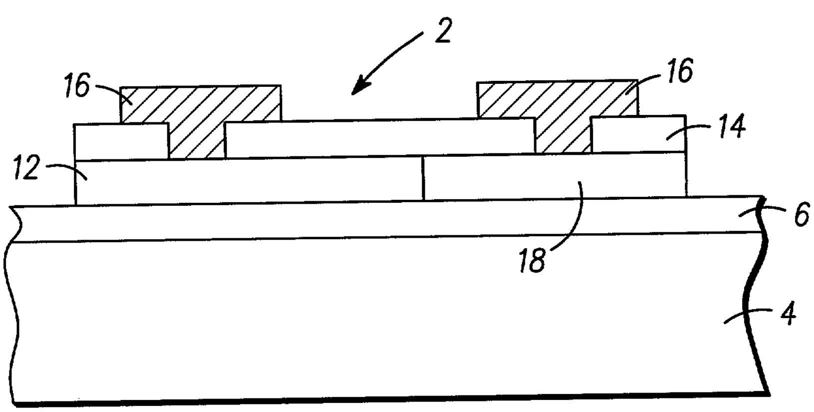

FIG. 4

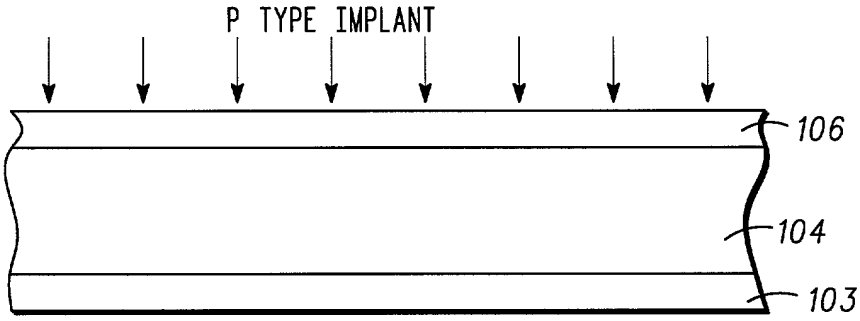

FIG. 5

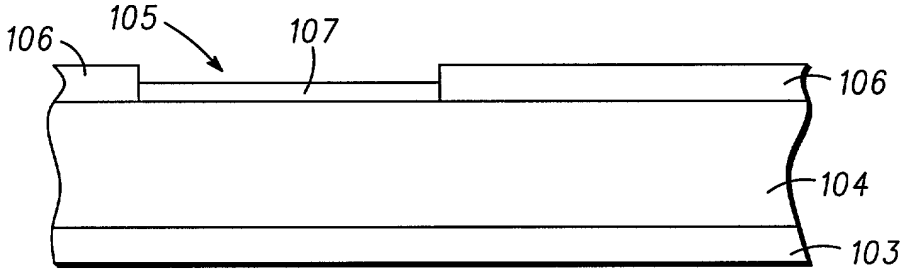

FIG. 6

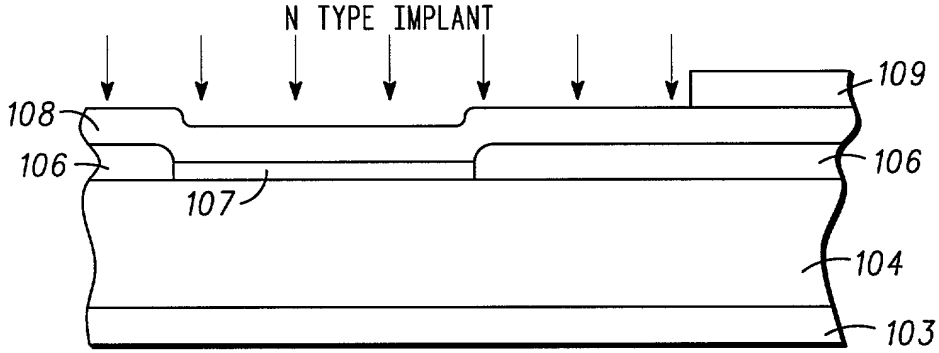

FIG. 7

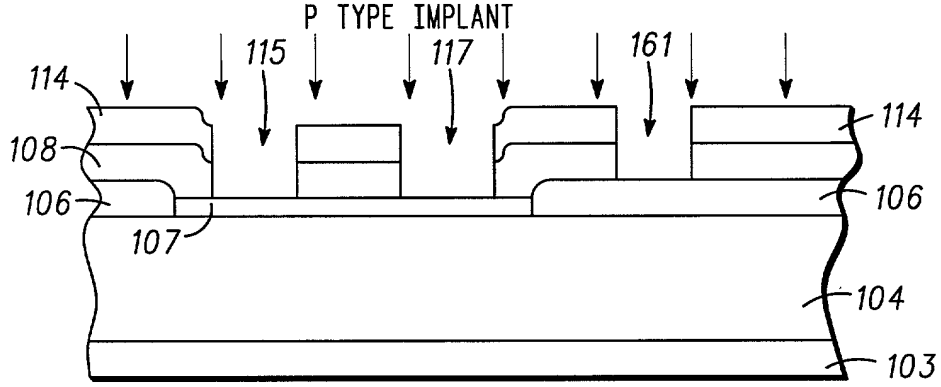

FIG. 8

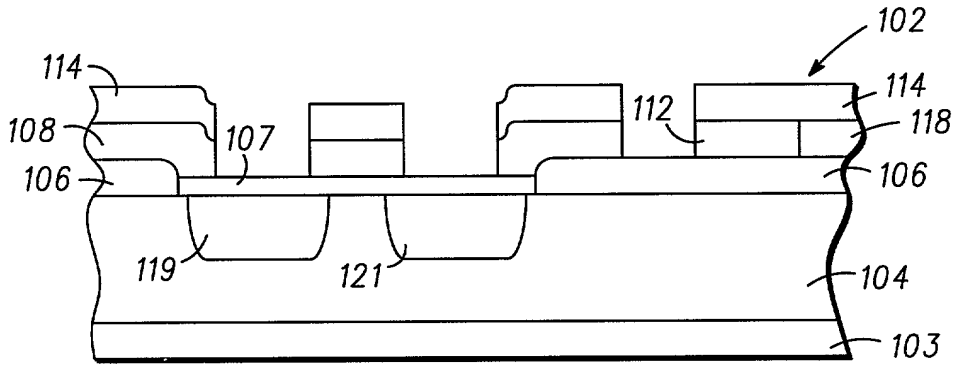

FIG. 9

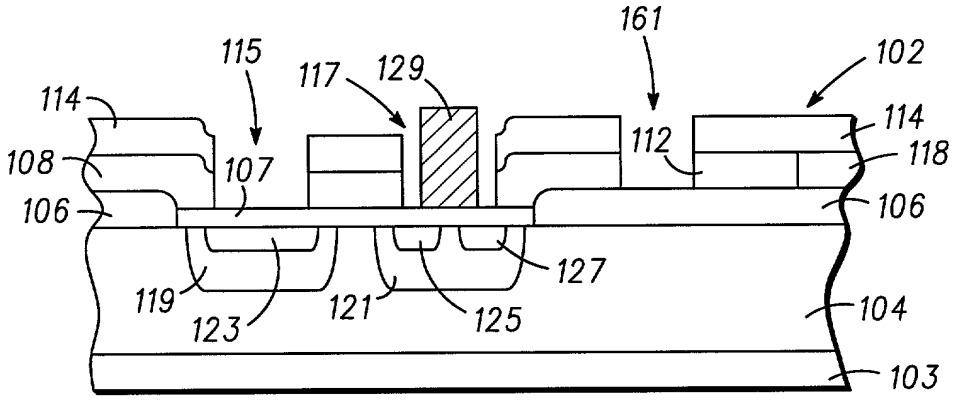

FIG. 10

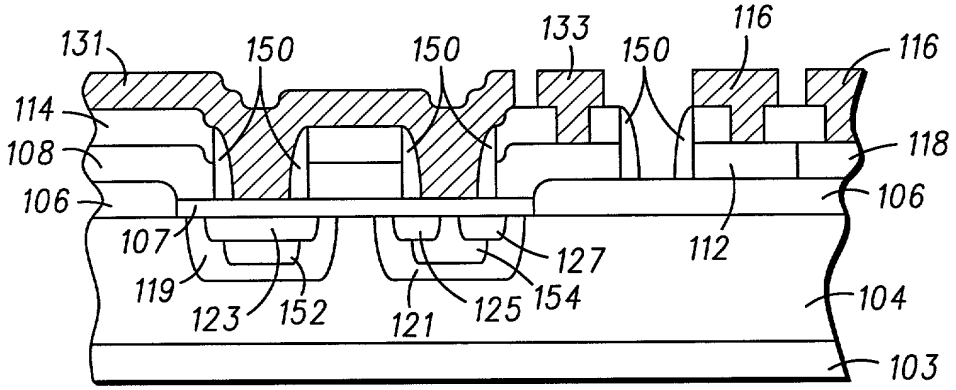

FIG. 11

COMBINED DECLARATION AND POWER OF ATTORNEY FOR PATENT APPLICATION

Attorney Docket SC0822ET

As a below named inventor, I hereby declare that:

My residence, post office address and citizenship are as stated below next to my name.

I believe I am the original, first and sole inventor (if only one name is listed below), or an original, first and joint inventor (if plural names are listed below), of the subject matter which is claimed and for which a patent is sought on the invention entitled METHOD OF FORMING A DIODE FOR INTEGRATION WITH A SEMICONDUCTOR DEVICE AND METHOD OF FORMING A TRANSISTOR DEVICE HAVING AN INTEGRATED DIODE, the specification of which is attached hereto unless the following line is marked:

____ Application was filed on _____
as Application No. _____
and was amended on _____.

I hereby state that I have reviewed and understand the contents of the above identified specification, including the claims, as amended by any amendment referred to above.

I acknowledge the duty to disclose information which is material to the patentability of this application in accordance with 37 C.F.R. §1.56.

I hereby claim foreign priority benefits under 35 U.S.C. §119(a)-(d) of any foreign application(s) for patent or inventor's certificate listed below and have also identified below any foreign application for patent or inventor's certificate having a filing date before that of the application on which priority is claimed.

Prior Foreign Application(s)			Priority Claimed
99402846.2	EPC	November 17, 1999	X Yes ___ No
(Number)	(Country)	(Day/Month/Year Filed)	
_____	_____	_____	___ Yes ___ No
(Number)	(Country)	(Day/Month/Year Filed)	

I hereby claim the benefit under 35 U.S.C. §119(e) of any United States provisional application(s) listed below.

_____	_____
(Application Number)	(Filing Date)
_____	_____
(Application Number)	(Filing Date)

Express Mail Label No. EL581727333US

I hereby claim the benefit under 35 U.S.C. §120 of any United States application(s) listed below and, insofar as the subject matter of each of the claims of this application is not disclosed in the prior United States application in the manner provided by the first paragraph of 35 U.S.C. §112, I acknowledge the duty to disclose information which is material to patentability as defined in 37 C.F.R. §1.56 which became available between the filing date of the prior application and the national or PCT international filing date of this application.

(Application Number)	(Filing Date)	(Status - patented, pending, abandoned)
(Application Number)	(Filing Date)	(Status - patented, pending, abandoned)

I hereby appoint the following attorney(s) and/or agent(s) to prosecute this application and to transact all business in the Patent and Trademark Office connected therewith:

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Direct all telephone calls to Mr. Mark D. Patrick at telephone no. (512) 996-6839.

Address all correspondence to Motorola, Inc., Austin Intellectual Property Law Section, 7700 West Parmer Lane, MD: TX32/PL02, Austin, Texas 78729.

I hereby declare that all statements made herein of my own knowledge are true and that all statements made on information and belief are believed to be true; and further that these statements were made with the knowledge that willful false statements and the like so made are punishable by fine or imprisonment, or both, under Section 1001 of Title 18 of the United States Code and that such willful false statements may jeopardize the validity of the application or any patent issued thereon.

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POST OFFICE ADDRESS.		
Same as above		

FULL NAME OF SECOND INVENTOR:	INVENTOR'S SIGNATURE	DATE:
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RESIDENCE.		CITIZENSHIP:
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POST OFFICE ADDRESS: Same as above		

FULL NAME OF THIRD INVENTOR·	INVENTOR'S SIGNATURE	DATE:
Evgueniy Stefanov		
RESIDENCE:		CITIZENSHIP:
10 Impasse Lascaux Appt. 58, 31500 Toulouse, France		France
POST OFFICE ADDRESS. Same as above		